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A Comparative Performance Analysis of Various CMOS Design Techniques for Multiplier Circuits

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Abstract: Multiplication is an important arithmetic operation that plays specific role in digital signal processing, microprocessors and scientific applications. Multipliers have become area of interest these days to search out high speed, low power consumption and area efficient multiplication algorithms. The Power- Delay product plays an effective role in overall performance of a multiplier. There are various low power digital designing techniques available to design digital multipliers. In this article various logic design techniques are used to design multipliers. As different CMOS technologies have different features, however new comparisons have been performed for efficient designing of binary multipliers. In this paper, 4-bit multipliers and 8-bit multipliers have been designed using various logic styles. The performance of both the multipliers have been compared and evaluated at different voltages on the basis of power consumption, area usage, cost applied and delay.

Keywords: CMOS, CPL, DPL, Full Adders, Logic design, Multipliers

I. INTRODUCTION

The arithmetic operations are widely used in many applications like microprocessors, portable IC devices, digital signal processing [1]. The very basic building blocks of any arithmetic circuits are adders and multipliers. Binary multipliers are the recurrently used components in most of the digital circuit models. However, with the rise in need of the low power, high speed, less delay portable devices, research work has been initiated to meet all these requirements [2]. The one of the frequently used basic operation of arithmetic circuits is multiplication. Extremely high speed multiplication is the demand of highly advanced digital models to fulfill the needs of complex mathematical applications [3]. The techniques that are involved in the designing of an arithmetic circuit undergo different steps. First step involves the selection of algorithm to be implemented. Then the next step precedes the designing at the architectural level [4]. Furthermore steps involves the circuit designing and last one is the system designing. One of the most important factors in designing of a multiplier is the power that circuit consumes [5]. Therefore power consumption defines the overall circuit performance. Also the transistors count plays a very crucial role in specifying system's cost. There are various types of multipliers that can be realized using different CMOS technologies [6].

In this paper, performance of the various techniques like CPL, DPL, and CSL based multiplier circuits were evaluated and compared. It was observed that the CPL technology based multiplier circuits consumed less number of transistors as compared to other techniques. The other two styles i.e. CSL & DPL based circuits have been implemented using more number of transistors.

The remaining part of this paper is organized as follow. Section II provides the short introduction to the Multipliers and it's designing. In Section III various designing algorithms are described. Section IV describes the Power dissipation & its types. Results of quantitative comparisons based on simulations of different design techniques are shown in Section V. Finally in Section VI some conclusions are made.

II. MULTIPLIERS & ITS DESIGNING

The multipliers play a crucial role in arithmetic operations in VLSI applications [7]. Low power designing has become the main issue in the development of multiplier circuits and digital processors [8]. The multipliers are widely used in Arithmetic and Logic Unit, DSP applications, filters, arithmetic processors and floating point circuits. There is tremendous increase in the demand of area efficient multipliers [9].

Using different styles of designing algorithms, various types of multipliers can be designed i.e. CPL, DPL & CSL. At structural level, the multipliers can be designed using array structures & tree structures [10]. So, there can be several methods of designing a multiplier circuit. In this paper the comparison of array and tree multipliers are shown designed using different logic styles [11].

A. Array Multipliers

An Array multiplier is very unvarying design [12]. The array multiplier originates from multiplication parallelogram [13]. Every partial product bit is fed into a full adder which sums the partial product bit with the sum from the previous adder and a carry from the less significant previous adder [14]. The number of rows in array multiplier denotes length of the multiplier and width of each row denotes width of multiplicand. The output of each row of adders acts as input to the next row of adders [15]. Each row of full adders or 3:2 compressors adds a

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partial product to the partial sum, generating a new partial sum and a sequence of carries as shown in Fig.2 [16].

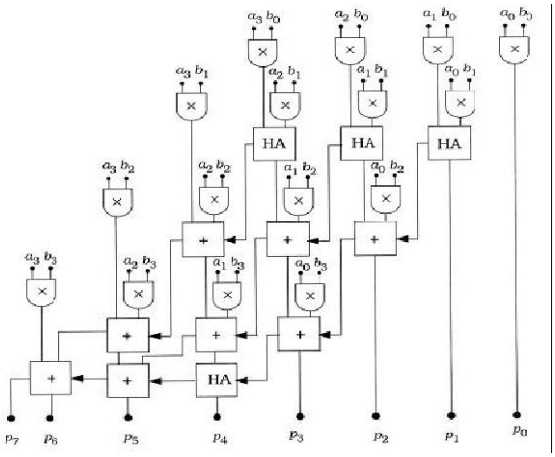

Fig.2. 4- bit Unsigned Array Multiplier Architecture

B. *Tree Multipliers*

Trees are an extremely fast structure for summing partial-products [17]. An efficient designing process for multiplication of two numbers was investigated by Wallace in1964 [18]. The main feature of this design is its approach towards execution of the circuit [19]. In tree multiplier partial-sum adders are arranged in a treelike fashion, reducing both the critical path and the number of adders needed as shown in the figure 3 [20].Schematic diagram of unsigned Tree Multiplier is shown in Fig.3.

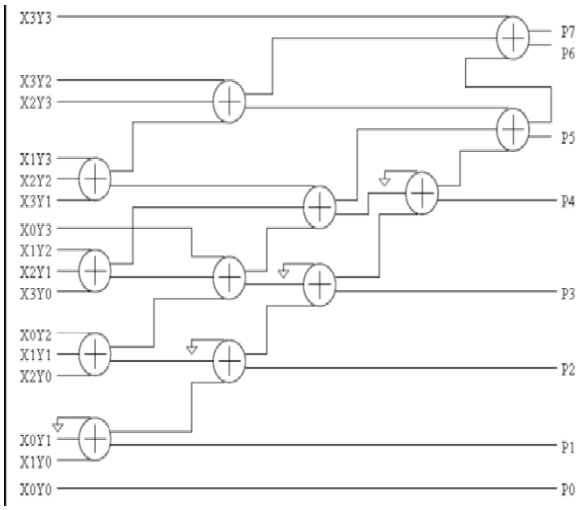

Fig.3. 4- bit Unsigned Tree Multiplier Architecture

III. VARIOUS DESIGNING ALGORITHMS

In low power design there are a variety of considerations like power dissipation due to hazards and critical race conditions, leakage and direct path currents, power consuming transitions in unused circuitry and pre-charge transistors. Description of some designing techniques is discussed in next subsections.

A. *Conventional Static CMOS Logic-CSL*

Conventional static CMOS [21] logic is used in most chip designs in VLSI applications [22]. CMOS is also defined as Complementary symmetry metal–oxide–semiconductor. The features of this logic style are good noise margin, fast speed and low power. The disadvantage of conventional static CMOS circuits is the voltage swing at the output nodes is equal to the supply voltage that results in higher power dissipation.

B. *Complementary Pass-Transistor logic- (CPL)*

CPL does not use pairs of two metal oxide semiconductor field effect transistors for the accomplishment of the low power logic functions [23]. It utilizes only one type of MOSFETs that is N-type MOSFETs. This is the reason that by implementing CPL techniques, the circuits will have high operating speed. It also includes an NMOS pass transistor logic network, and CMOS output inverters

C. *Double Pass-transistor Logic- DPL*

DPL is a modified version of CPL. In DPL circuits, full voltage swing is achieved at outputs by adding a PMOS transistor in parallel with NMOS transistors.
The features of this logic style are low power consumption, complimentary inputs and outputs. Other advantage of DPL is that this technique eliminates the need for restoration circuitry. Also, this technique has reduced delay as compared to the CPL and CSL techniques.

D. *Gate-Diffusion Input - (GDI)*

Gate diffusion input (GDI) - a new technology of low-power digital combinational designing of circuits - is presented in 2001[24]. GDI technology provides the designing of low power circuits and having low propagation delay. The GDI method is based on the use of a simple cell as shown in Fig. 4.

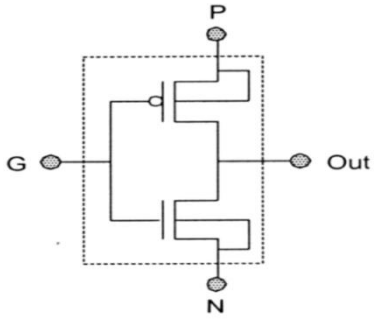

Fig.4. Basic GDI cell

IV. POWER DISSIPATION AND ITS TYPES

The Power dissipation is the most critical parameter for portability & mobility [25]. It is classified in to Dynamic and Static power dissipation. Dynamic power dissipation arises when the circuit is operational, while static power dissipation becomes an issue when the circuit is inactive or is in a power-down mode [26].

V. PERFORMANCE PARAMETERS AND SIMULATION SET-UP

The different multipliers are compared based on the performance parameters like propagation delay, number of transistors and power dissipation. To achieve better

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performance, the circuits are designed using CMOS process by EDA TANNER in 180nm technology.

In Figure 5, 6, & 7 the comparison of transistor count, power consumption & delay in implementing 4-bit multipliers (array & tree) using various technique is shown using graphical representation.

In figures 8, 9 &10 the comparison for 8-bit multipliers has been shown using graphical representation.

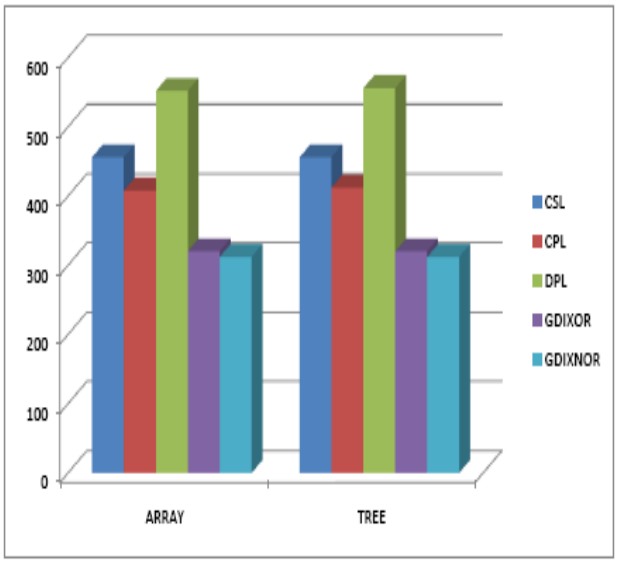

Fig.5. Comparison of transistor count in 4-bit multiplier (array & tree) for various logic designs.

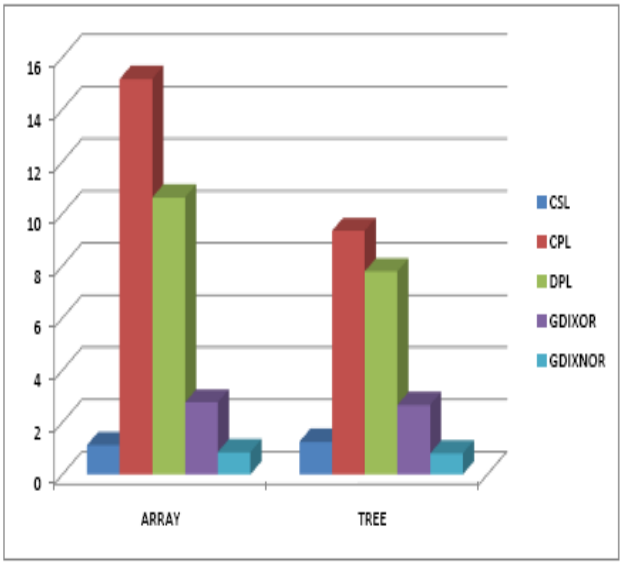

Fig.6. Comparison of power consumption in 4-bit multiplier (array & tree) for various logic designs.

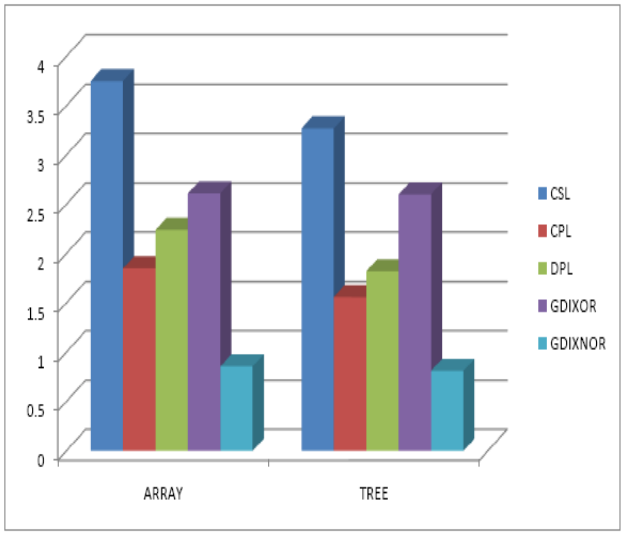

Fig.7. Comparison of delay in 4-bit multiplier (array & tree) for various logic designs.

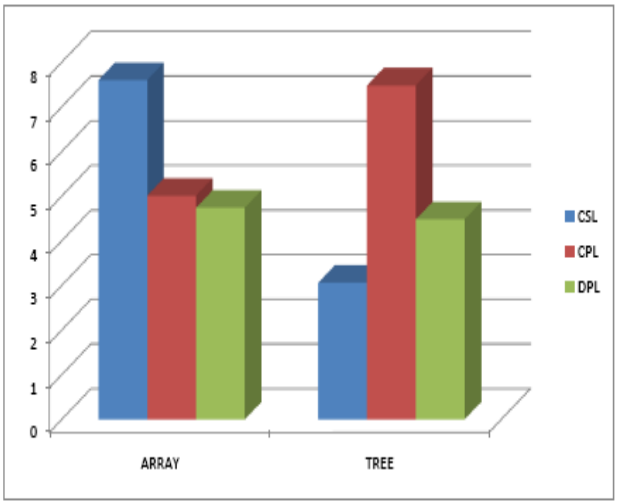

Fig.8. Comparison of power consumption in 8-bit multiplier (array & tree) for various logic designs.

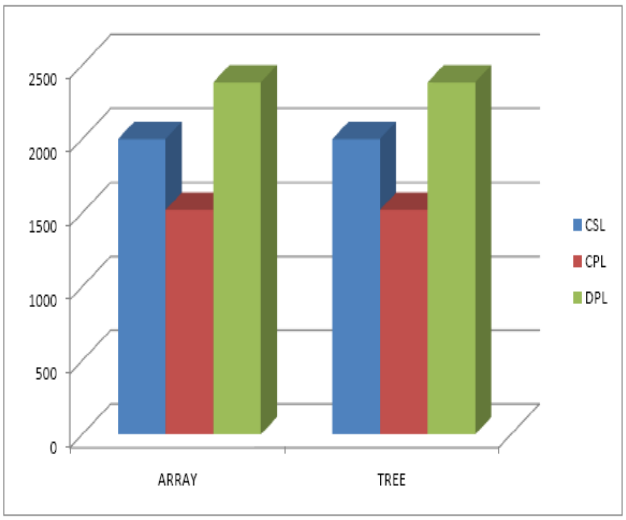

Fig.9. Comparison of transistor count in 8-bit multiplier (array & tree) for various logic designs.

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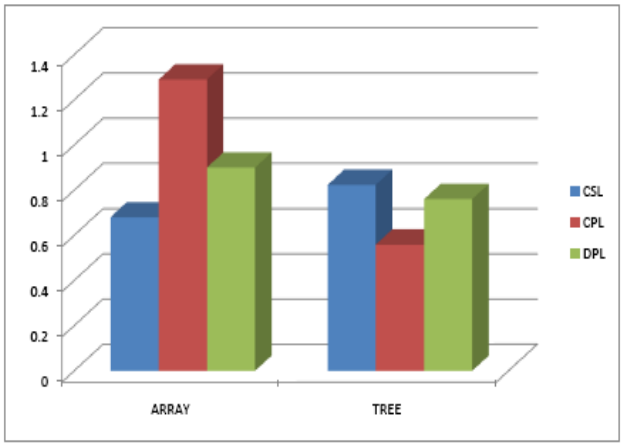

Fig.10. Comparison of delay in 8-bit multipliers (array & tree) for various logic designs.

VI. CONCLUSION

All the circuits have been implemented on the basis of requirement of different applications. Different logic styles have been proved to be efficient in various applications like most of the functions are complex in CMOS, but very simple (only two transistors per function) in the GDI design method. Here, we have compared some features of different logic styles. The CPL logic style has performed better in case of delay induced and area usage as compared to other logic designs. So, CPL logic style can be used where portability and high speed is the prime aim. Where, CSL consumes the lowest power among the three. But, the CPL logic design style has propagation delay comparable to DPL and CSL logic design style, so CPL can be considered best logic design style with respect to all parameters of 4-bit & 8-bit multiplier (array & tree) architectures.

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